1. A method of fabricating an integrated circuit seal ring comprising:

providing an active area including semiconductor device structures; and

forming a continuous conductive loop around the perimeter of said integrated circuit whereby said conductive loop has a plurality of sections having at least two different alternating widths, wherein said conductive loop forms said seal ring.

2. The method according to Claim 1 wherein the narrowest of said different alternating widths is between about 0.5 and 50 μm.

3. The method according to Claim 1 wherein the widest of said different alternating widths is between about 1 and 55 μm.

4. The method according to Claim 1 whereby the characteristic impedance of each of said different alternating widths is different.

5. A method of fabricating an integrated circuit seal ring comprising:

providing an active area including semiconductor device structures; and

forming a continuous conductive loop around the perimeter of said integrated circuit by patterning and forming a plurality of stacked, interconnected, conductive layers whereby said conductive loop has a plurality of sections having at least two different alternating widths, wherein said conductive loop forms said seal ring.

6. The method according to Claim 5 wherein the narrowest of said different alternating widths is between about 0.5 and 50 μm.

7. The method according to Claim 5 wherein the widest of said different alternating widths is between about 1 and 55 μm.

8. The method according to Claim 5 whereby the characteristic impedance of each of said different alternating widths is different.

9. A method of fabricating an integrated circuit seal ring comprising:

providing an active area including semiconductor device structures; and

forming a continuous conductive loop around the perimeter of said integrated circuit by patterning and forming a plurality of stacked, interconnected, conductive layers whereby said conductive loop has a plurality of sections having at least two different alternating widths and each of said conductive layers is formed by steps comprising:

depositing an inter-metal dielectric layer;

etching openings through said inter-metal dielectric layer;

filling said openings with a conductive via layer; and

depositing and patterning a conductive metal layer to make contact to said conductive via layer filling said openings in said inter-metal dielectric layer, wherein a first of said conductive via layers makes electrical contact to signal ground points within the substrate of said active area, and wherein each of subsequent said conductive via layers makes electrical contact to previous patterned said conductive metal layer, completing fabrication of said integrated circuit seal ring.

10. The method according to Claim 9 wherein the narrowest of said different alternating widths is between about 0.5 and 50 μm.

11. The method according to Claim 9 wherein the widest of said different alternating widths is between about 1 and 55 μm.

12. The method according to Claim 9 whereby the characteristic impedance of each of said different alternating widths is different.

13. A seal ring surrounding the perimeter of an integrated circuit comprising at least two different and alternating conductive transmission lines, each having a different characteristic impedance.

14. The seal ring according to Claim 13 wherein said different and alternating transmission line sections comprise a plurality of stacked, interconnected, conductive layers.

15. The seal ring according to Claim 13 wherein said different and alternating transmission line sections comprise a plurality of stacked, interconnected, conductive layers forming a conductive loop, whereby said conductive loop has a plurality of sections having at least two different alternating widths.

16. The seal ring according to Claim 13 wherein the width of the narrowest of said different and alternating transmission line sections is between about 0.5 and 50

17. The seal ring according to Claim 13 wherein the width of the widest of said different and alternating transmission line sections is between about 1 and 55 μm.

18. The seal ring according to Claim 13 whereby the characteristic impedance of each of said different and alternating transmission line sections is different.

19. The seal ring according to Claim 13 wherein said different and alternating transmission line sections are fabricated by forming a plurality of stacked, interconnected, conductive layers each of which is formed by steps comprising:

depositing an inter-metal dielectric layer;

etching openings through said inter-metal dielectric layer;

filling said openings with a conductive via layer; and

depositing and patterning a conductive metal layer to make contact to said conductive via layer filling said openings in said inter-metal dielectric layer, wherein a first of said conductive via layers makes electrical contact to signal ground points within the substrate of said active area, and wherein each of subsequent said conductive via layers makes electrical contact to previous patterned said conductive metal layer, completing said integrated circuit seal ring.

20. The seal ring according to Claim 19 wherein the width of said conductive metal layers of the narrowest of said different and alternating transmission line sections is between about 0.5 and 50 μm.

21. The seal ring according to Claim 19 wherein the width of said conductive metal layers of the widest of said different and alternating transmission line sections is between about 1 and 55 μm.

22. The seal ring according to Claim 19 wherein the width of said via layers of the narrowest of said different and alternating transmission line sections is between about 0.5 and 50 μm.

23. The seal ring according to Claim 19 wherein the width of said via layers of the widest of said different and alternating transmission line sections is between about 1 and 55 μm.